21. A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface.

22. The semiconductor device in claim 21, wherein a bottom 80% to 90% of said bonding pad is free of silicide.

23. The semiconductor device in claim 22, wherein said silicided surface is free of oxides and silicide islands.

24. The semiconductor device in claim 23, wherein, prior to formation of said silicided surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen plasma to make said bonding pad free of said oxides and silicide islands.

25. The semiconductor device in claim 21, further comprising a terminal connected to said bonding pad, wherein a thickness of said silicided surface increases adhesion between said terminal and said bonding pad.

26. The semiconductor device in claim 25, wherein said terminal comprises one of a lead and tin solder.

27. The semiconductor device in claim 21, further comprising at least one internal level of metallurgy within an interior of said semiconductor device, wherein said top level of metallurgy is thicker than said internal level of metallurgy.

28. The semiconductor device in claim 21, wherein said top level of metallurgy comprises copper.

29. A semiconductor chip comprising:
an exterior surface having a top level of metallurgy; and
an interior having at least one internal level of metallurgy,
wherein said top level of metallurgy is thicker than said internal level of metallurgy,
wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and
wherein an upper 10% to 20% of said bonding pad comprises a silicided surface.

30. The semiconductor device in claim 29, wherein a bottom 80% to 90% of said bonding pad is free of silicide.

31. The semiconductor device in claim 30, wherein said bonding pad is free of oxides and silicide islands.

32. The semiconductor device in claim 31, wherein, prior to formation of said silicided surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen plasma to make said bonding pad free of said oxides and silicide islands.

33. The semiconductor device in claim 29, further comprising a terminal connected to said bonding pad, wherein a thickness of said silicided surface increases adhesion between said terminal and said bonding pad.

34. The semiconductor device in claim 33, wherein said terminal comprises one of a lead and tin solder.